**Muffakham Jah College of Engineering and Technology**

**Sultan-ul-uloom Education society**

**Banjara Hills, Road No. 3**

**ELECTRONICS AND COMMUNICATION ENGINEERING DEPARTMENT**

**COMPUTER ORGANIZATION AND ARCHITECTURE- PC505EC**

**CLASS TEST-2**

**V SEMESTER (2019-2020)**

**NOTE: ANSWER ALL QUESTIONS FROM PART-A and ANY TWO**

**QUESTIONS FROM PART-B.**

**ANY MISSED DATA CAN BE ASSUMED APPROPRIATELY.**

**CO3: Understand I/O interfacing of a computer**

**CO4: Interface microprocessor with memory devices**

**CO5: Understand latest trends in microprocessors**

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**Time: 1 Hr. Max.Marks: 20**

**PART – A**

1. Determine the number of clock cycles that it takes to process 100 tasks in a five-segment pipeline. [CO3] (2M)
2. Why does DMA have priority over the CPU when both request a memory transfer?   
    [CO4] (2M)
3. What do you mean by a page fault? Which hardware is responsible for detecting the page fault? [CO5] (2M)

**PART – B**

1. Write a brief note on the following: [CO3]

i) Comparison between CISC and RISC (4M)

ii) Array processors (3M)

1. What are the disadvantages of transferring data through strobe control method? How handshaking overcomes this disadvantage? Explain. [CO4] (7M)
2. What are the cache design elements? Explain set-associative cache mapping in   
    cache memory. [CO5] (7M)

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| **Class Test Q.No.** | **1** | **2** | **3** | **4** | **5** | **6** |
| **Marks (Xi)** | **2** | **2** | **2** | **7** | **7** | **7** |
| **Bloom’s Score (Si)** | **3** | **4** | **2** | **4** | **3** | **4** |
| **Xi\*Si** | **6** | **8** | **4** | **28** | **21** | **28** |

**BI=4.75**